

AMENDMENTS TO THE CLAIMS

1. (Currently amended) A phase frequency detector comprising:
 - a phase error detecting unit for outputting at least a phase error signal according to a phase error between a first input signal and a second input signal; and
 - a reset unit coupled to the phase error detecting unit for receiving the first input signal and the second input signal, and for outputting ~~a reset signal~~ ~~reset signals~~ according to the first input signal and the second input signal, in order to reset the phase error detecting unit;
wherein the phase error detecting unit comprises:
 - a first flip-flop for outputting a first flag signal according to the first input signal;
 - a second flip-flop for outputting a second flag signal according to the second input signal; and
 - a sampling circuit for outputting the phase error signal according to the first flag signal and the second flag signal;
wherein the length of the phase error signal has a substantial linear relationship with the phase error of the first input signal and the second input signal;
wherein the phase error detecting unit is reset by the reset signal responsive to an edge of the first input signal, and remains reset for a significant period of time despite of the level of the first input signal after said edge.

2. (Original) The phase frequency detector according to claim 1, wherein the phase error signal comprises a first output signal and a second output signal.

3. (Canceled)

4. (Canceled)

5. (Currently amended) The phase error detector according to claim 1 3, wherein the time from a state transition of the first input signal to a corresponding reset of the phase error detecting unit is substantially the same as the time from the state transition of the first input signal to a corresponding state transition of the first flag signal.

6. (Currently amended) The phase frequency detector according to claim 1 3, wherein the reset signals comprise:

a first reset signal for resetting the first flip-flop; and
a second reset signal for resetting the second flip-flop.

7. (Original) The phase frequency detector according to claim 6, wherein the reset unit comprises:

a third flip-flop for outputting the second reset signal according to the first input signal;
and
a fourth flip-flop for outputting the first reset signal according to the second input signal.

8. (Original) The phase frequency detector according to claim 1, wherein the phase error detecting unit further comprises a buffer circuit for buffering the first input signal and the second input signal.

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (New) A phase frequency detector comprising:

a phase error detecting unit for outputting at least a phase error signal according to a phase error between a first input signal and a second input signal; and

a reset unit coupled to the phase error detecting unit for receiving the first input signal and the second input signal, and for outputting a first reset signal and a second reset signal according to the first input signal and the second input signal, in order to reset the phase error detecting unit;

wherein the phase error detecting unit comprises:

a first flip-flop for outputting a first flag signal according to the first input signal;
and

a second flip-flop for outputting a second flag signal according to the second input signal;

wherein the first reset signal resets the first flip-flop and the second reset signal resets the second flip-flop;

wherein the reset unit comprises:

a third flip-flop for outputting the second reset signal for resetting the second flip-flop according to the first input signal; and

a fourth flip-flop for outputting the first reset signal for resetting the first flip-flop according to the second input signal;

wherein the length of the phase error signal has a substantial linear relationship with the phase error of the first input signal and the second input signal;

wherein the phase error detecting unit is reset by the reset signal responsive to an edge of the first input signal, and remains reset for a significant period of time despite of the level of the first input signal after said edge.

15. (New) The phase frequency detector according to claim 14, wherein the phase error signal comprises a first output signal and a second output signal.

16. (New) The phase frequency detector according to claim 15, wherein the phase error detecting unit further comprises a sampling circuit for outputting the first output signal and the second output signal according to the first flag signal and the second flag signal.

17. (New) The phase frequency detector according to claim 14, wherein the phase error detecting unit further comprises a buffer circuit for buffering the first input signal and the second input signal.

18. (New) The phase error detector according to claim 14, wherein the time from a state transition of the first input signal to a corresponding reset of the phase error detecting unit is substantially the same as the time from the state transition of the first input signal to a corresponding state transition of the first flag signal.